CLAIMS

We claim:

1. A system for handling data for data processing means utilizing a plurality of memory registers comprising:

a first multiplexor means for receiving data from said processing means coupled to said memory registers;

a second multiplexor means for outputting data from said memory means coupled to said memory registers;

a plurality of registers configured into slices of arrays, each slice having two independent inputs coupled to said first multiplexor means to receive data input from said first multiplexor means and each slice having two independent outputs to convey data to said second multiplexor means;

means to track the identification and location of data being stored to said registers from said first multiplexor means;

means to select identified data within said register means for output to said second multiplexor means.

2. The system of claim 1 further including means to forward said identified data to a requested destination within said processing means.

3. The system of claim 1 wherein said first multiplexor means comprises eight ports coupled to said register means.

4. The system of claim 1 wherein said second multiplexor means comprises eight ports coupled to the output of said register means.

5. The system of claim 1 wherein said first multiplexor means comprises a four to one multiplexor.

6. The system of claim 5 wherein said second multiplexor means comprises a one to four multiplexor.

7. The system of claim 1 wherein further said plurality of registers are such that a memory access by the system can be overlapped with a data transfer.

8. The system of claim 1 wherein said plurality of registers is comprised of an array of eight separate 72 bit memory registers, configured into four slices, whereby each slice is comprised of two said memory registers operatively connected to store 64 lines of four 144- bit data words in each said slice, each said register having at least one input port.

9. A method of handling data between a central processing unit (CPU) and a data storage means in which the data storage means receives and stores a continuous flow of data items being processed in the CPU in which data items are received from multiple sources simultaneously comprised of a plurality of memory registers configured into an array of four slices of memory, each slice having two input ports coupled to an input multiplexor means and two output ports coupled to an output multiplexor means, the method comprising the steps of:

providing data words from said CPU to a first multiplexor interface means coupled to said CPU and said memory;

identifying and tracking each said data word;

storing said data words sequentially in each slice of memory and storing the location and identification of each data word stored;

outputting said data words to a destination requested by said CPU by identifying and selecting the slice containing the start of the requested data and sequentially reading the data words requested.

10. A method of handling data between a central processing unit (CPU) and a data storage means in which the data storage means receives and stores a continuous flow of data items being processed in the CPU in which data items are received from multiple sources simultaneously comprised of a plurality of memory registers configured into an array of four slices of memory, each slice having two input ports coupled to an input multiplexor means and two output ports coupled to an output multiplexor means, the method comprising the steps of:

a. looking up data requested by the CPU in an auxiliary storage register which stores data location;

b. selecting the resulting data slice;

c. conveying said data slice to the destination requesting said slice based on a predetermined output order;

d. conveying said slice to the requested destination; and

e. continuing the steps of ***c*** and ***d*** until such requests are fulfilled.

11. The method of claim 10 wherein further if multiple destinations request the same data slice, the conveyance of said data slice to the requested destination is in the order of:

designated high priority output slices;

previously held pre-empted data transfers of said data slices;

then previous data slices in accordance with (n - 1) wherein n equals the previously preempted slice until all previously preempted slices are conveyed; and

any new data transfer request selected from multiple requests for data from said CPU.

12. A method of increasing data handling speed in a computer memory system utilizing random access memory arrays arranged in at least two slices of memory registers handling data from multiple input sources or output destinations comprising the steps of:

providing data from the computer system processor to a multiplexor means coupled to said processor and said memory, wherein said multiplexor means continuously selects said memory registers sequentially;

sequentially storing data from said first multiplexor means beginning at any data storage line within any said slice;

identifying the location of the first said storage line of data in each said slice and storing such location information;

outputting data from said memory registers when requested to a destination by reading the location of the starting slice of the requested data and reading such data sequentially beginning at said starting slice.

13. Apparatus for handling data in a data processing system, comprising:

first and second memories, each having an input for writing data into the memory and an output for reading the data from the memory;

a first input multiplexor having multiple system inputs for receiving the data, and an output coupled to the input of the first memory;

a second input multiplexor having multiple system inputs for receiving the data simultaneously with the first input multiplexors receiving the data, and an output coupled to the input of the second memory;

an output multiplexor having inputs coupled to the outputs of the first and second memories;

an input controller including identification and location of the data in the memories; and

an output controller responsive to the identification and location of the data, and coupled to the output multiplexor.

14. The apparatus of claim 13 wherein the data received by the first multiplexor does not equal that of the second.

15. The apparatus of claim 13 wherein the first and second memories each have second inputs.

16. The apparatus of claim 15 further including third and fourth input multiplexors, each having multiple system inputs for receiving second data, an output of the third input multiplexor being coupled the second input of the first memory, and an output of the fourth input multiplexor being coupled the second input of the second memory.

17. The apparatus of claim 16 wherein the second data is not equal to the data of first and second multiplexor.

18. The apparatus of claim 13 wherein the first and second memories each have second outputs.

19. The apparatus of claim 18 further including a second output multiplexor having inputs coupled to the second outputs of the first and second memories.

20. The apparatus of claim 19 wherein the second output multiplexor is active simultaneously with the first output multiplexor.

21. The apparatus of claim 13 wherein the first output multiplexor has an output coupled to a first system output, and further including a second output multiplexor having inputs coupled to the outputs of the first and second memories and an output coupled to a second system output.

22. The apparatus of claim 13 further including third and fourth memories.

23. The apparatus of claim 13 further including additional memories, wherein the number of memories is equal to the number of words in a unit of storage of the data.

24. The apparatus of claim 13 wherein each of the first and second memories comprises two or more memory elements, each memory element storing less than an entire word of each unit of storage of the data.